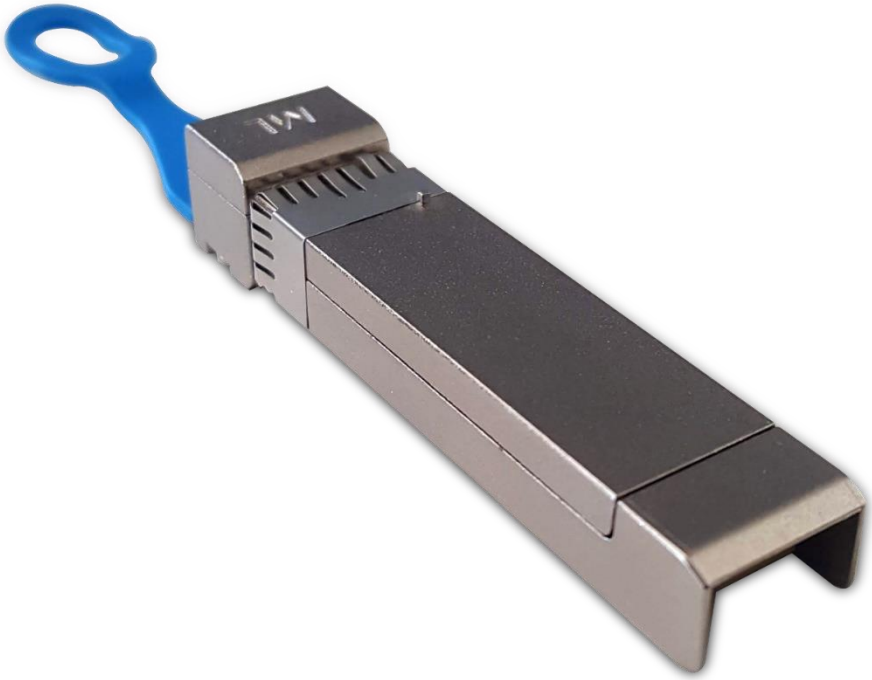
ML4022-LB-V3

MSA Compliant SFP-DD (MIS Rev2.0)

Electrical Passive Loopback



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Contents

Table of figures:

ML4022-LB-V3 Electrical Passive Loopback Interconnect - Key Features

- ✓ Power Consumption up to 4.96W, spread over 4 spots
- ✓ Dual channels, supporting up to 28 Gbaud each (56Gbps)
- ✓ LED indicator
- ✓ Custom Memory Maps
- ✓ Temperature range from 0° to 85° C
- ✓ I2C Interface
- ✓ MSA Compliant EEPROM
- ✓ Voltage sense
- ✓ Temperature sense
- ✓ Insertion Counter
- ✓ Micro controller based

LED Indicator

Green - Signifies that the module is operating in high power mode.
Red - Signifies that the module is operating in Low power mode.

Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.60	V
Data Rate	R_b	Guaranteed to work at 56 Gbps	0		56	Gbps
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0	-	4.96	W

Ordering Information

Multilane provides two different part numbers for the ML4022-LB-V3, differing in the power spots distribution and the maximum power dissipation. Ordering Part Numbers are described in the table below.

Part Number	Description
ML4022-LB-V3	Maximum power spots dissipation: 4.32W
ML4022-LB-5W-V3	Maximum power spots dissipation: 4.96W

1. General Description

The **ML4022-LB-V3** SFP-DD Passive Electrical Loopback is used for testing SFP-DD transceiver ports under board level tests. By substituting a full-featured SFP-DD transceiver with the **ML4022-LB-V3**, its electrical loopback provides a cost effective low loss method for SFP-DD port testing.

The **ML4022-LB-V3** is packaged in a standard MSA housing compatible with all SFP-DD ports. High speed signals are electrically looped back from TX side to RX side of the module, the differential TX pair is connected to the corresponding RX pair, and the signals are AC coupled as specified by SFP-DD MSA HW specs.

2. Functional Description

2.1 Serial Data Interface – I2C

The ML4022-LB-V3 supports the I2C interface.

2.2 I2C Signals, Addressing and Frame Structure

I2C Frame:

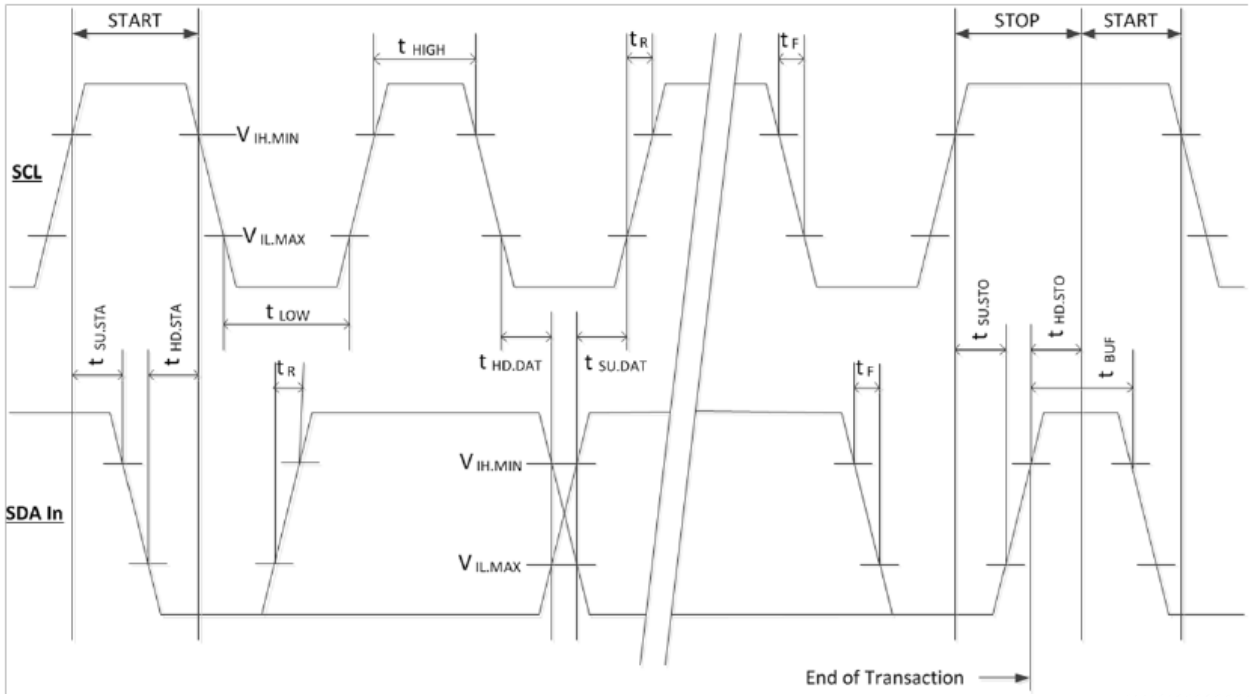

Figure 1: I2C Frame

The 2-wire serial interface address of the SFP-DD module is A0h.

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	0	400	kHz
Clock Pulse Width Low	t_{LOW}	1.3		us
Clock Pulse Width High	t_{High}	0.6		us

Time bus free before new transmission can start	t_{BUF}	20		us
Input Rise Time (400kHz)	$t_{R,400}$		300	ns
Input Fall Time (400kHz)	$t_{F,400}$		300	ns
Serial Interface Clock Holdoff "Clock Stretching"	T_{clock_hold}		500	us

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the SFP-DD in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host should be acknowledged by SFP-DD transceiver. Read data bytes transmitted by SFP-DD transceiver should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. If SFP-DD releases the bus, host is free to initiate a Start condition
4. If SDA remains low, TWI reset has failed

Device Addressing: SFP-DD devices require an 8-bit device address word following a start condition to enable a read or write operation. Data is transferred with the most significant bit (MSB) first.
The device address word consists of a mandatory sequence for the first seven most significant bits of device address (A0h). This is common to all SFP-DD devices.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low.

2.3 I2C Read/Write Functionality

2.3.1 SFP-DD Memory Address Counter (Read AND Write Operations)

SFP-DD devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as

long as SFP-DD power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

2.3.2 Read Operation

2.3.2.1 Current Address Read

A current address read operation requires only the device address read word (10100001) to be sent, see Figure 2.

		<--- CONTROL WORD --->																		
MASTER	START	MSB							LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE											ACK	MSB						LSB		
												<---- DATA WORD ----->								

Figure 2: SFP-DD Current Address Read Operation

Once acknowledged by the SFP-DD, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.2 Random Read

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 3 below. This is accomplished by the following sequence.

		<--CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL WORD -->																	
START	MSB						LSB	READ									NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									

Figure 3: SFP-DD Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the SFP-DD. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The SFP-DD acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.3 Sequential Read

Sequential reads are initiated by a current address read (Figure 4) or a random address read (Figure 5). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the SFP-DD receives an acknowledgement, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

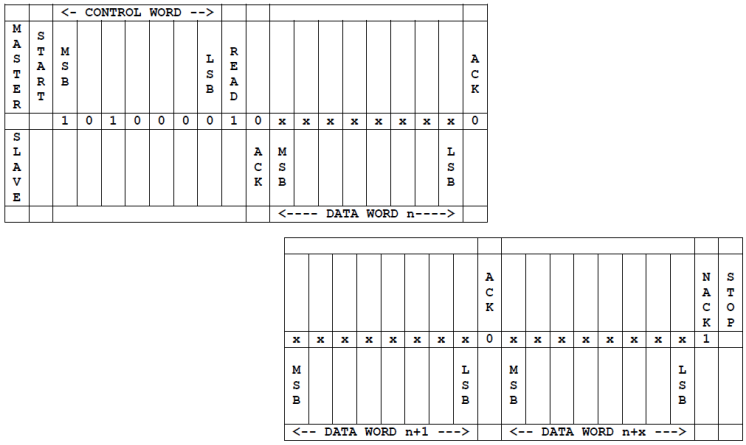

Figure 4: Sequential Address Read Starting at SFP-DD Current Address

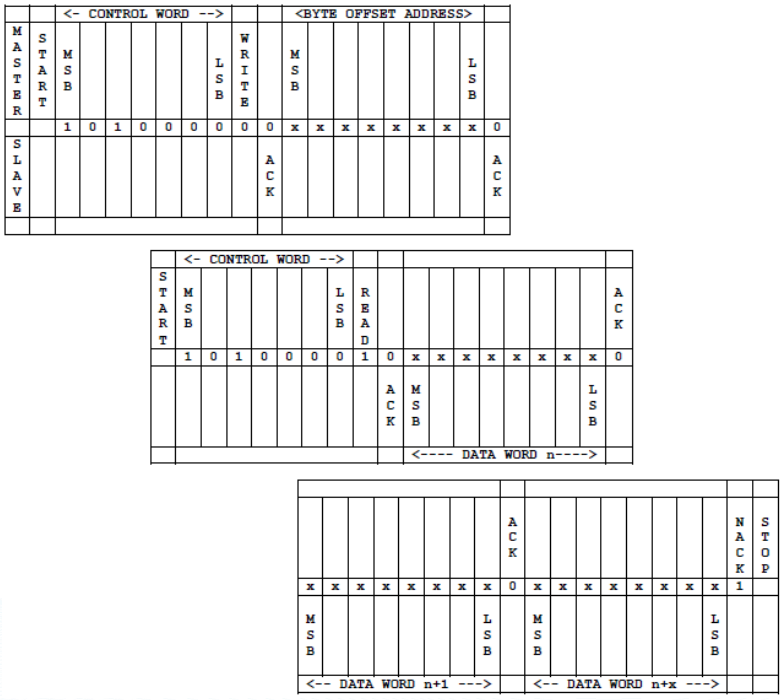

Figure 5: Sequential Address Read Starting at SFP-DD Random Address

2.3.3 Write operation

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement. Upon receipt of this address, the SFP-DD will again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the SFP-DD will output a zero (ACK) and the Host must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (repeated START) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the SFP-DD enters an internally timed write cycle to internal memory. The SFP-DD disables its management interface input during this write cycle and will not respond or acknowledge subsequent commands until the internal memory write is complete.

		<- CONTROL WORD -->								<BYTE OFFSET ADDRESS>								<- DATA WORD ->									
MASTER	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	X	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SLAVE										ACK									ACK									ACK	

Figure 6: SFP-DD Single Write Operation

2.3.3.1 Sequential Write

Sequential byte write of up to eight bytes without repeatedly sending slave address and memory address information is supported. In a sequential write, the host should not include in the sequence a mixture of volatile and non-volatile registers.

A sequential write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the SFP-DD acknowledges receipt of the first data word, the Host can transmit additional data words: seven additional words for non-volatile memory or volatile memory. The SFP-DD will send acknowledge after each data word received.

The Host must terminate the sequential write sequence with a STOP condition.

Upon receipt of the proper Stop condition, the slave may enter an internally timed write cycle to internal memory. If there is no proper STOP condition, the results of the sequential write are unpredictable.

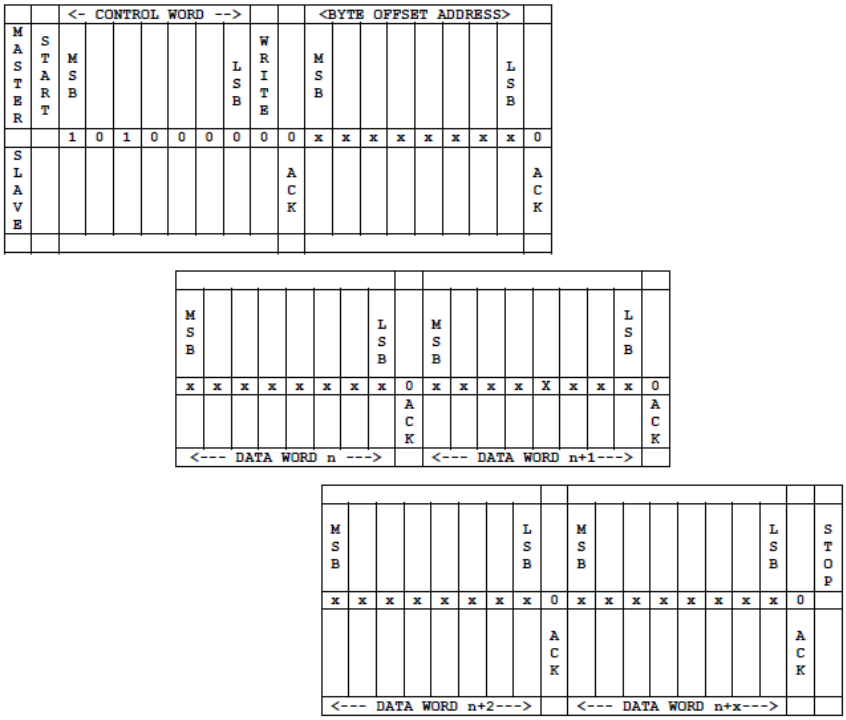

Figure 7: SFP-DD Sequential Write Operation

2.4 SFP-DD Memory Map

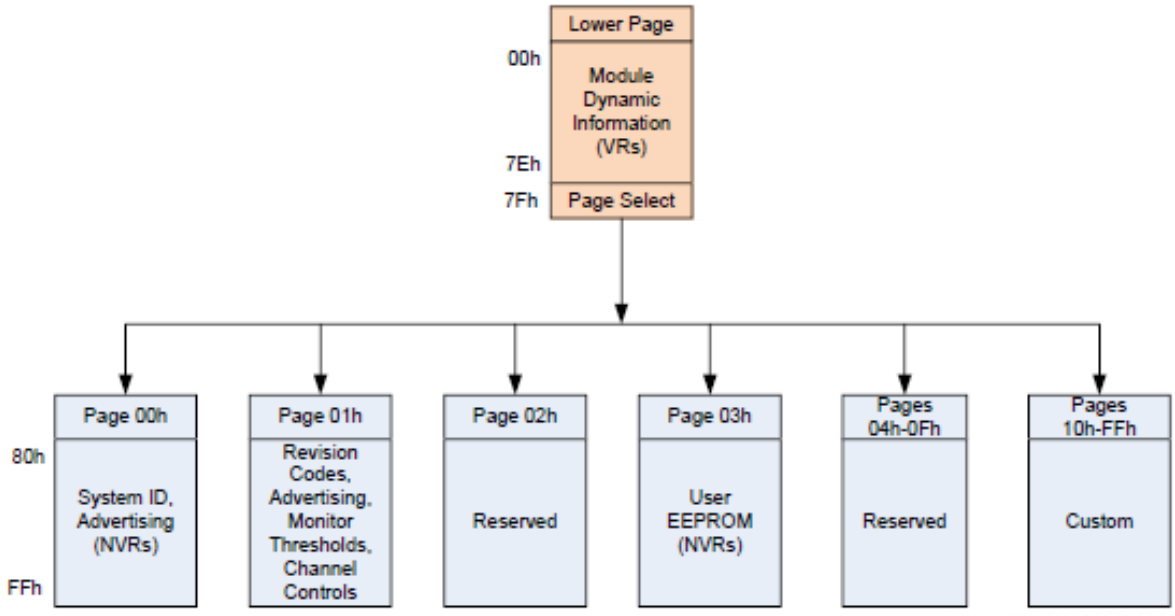

Figure 8: SFP-DD Memory Map

2.5 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- TxFault, IntL/TxFaultDD
- TxDisable, TxDisableDD
- LPMode
- Speed1, Speed2, Speed1DD, Speed2DD
- RxLOS, RxLOSDD
- MOD_ABS

2.5.1 TxFault

TxFault is a module output signal that when high, indicates that the module has detected a fault condition and has entered the Fault state. For testing purpose, the signal can be controlled by the user as detailed in section 2.6.4.

2.5.2 IntL/TxFaultDD

IntL/TxFaultDD is a dual function signal. It can be optionally configured for either IntL or TxFaultDD signal. By default, the signal is configured as IntL. After module is initialized the signal can be programmed over I2C, as detailed in section 2.6.3. When it is configured as IntL, a low state indicates a status critical to the host system. For testing purpose, the signal can be controlled by the user as detailed in section 2.6.4.

2.5.3 TxDisable/ TxDisableDD

TxDisable and TxDisableDD are module input signals. The signals are pulled up to VccT in the module through 12K Ohm resistors. The user can read the state of these signals as detailed in section 2.6.5.

2.5.4 LPMode

LPMode is a module input signal operating with active high logic. The LPMode signal is pulled up to Vcc in the module through 12 KOhm resistor. The LPMode signal state controls the power state of the module, as detailed in section 2.6.2.

2.5.5 Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module input signals. These signals are pulled-down to ground in the module through 56 KOhm resistors. The user can read the state of these signals as detailed in section 2.6.7.

2.5.6 RxLOS, RxLOSDD

RxLOS and RxLOSDD are output signals. When high it indicates a low data signal level. For testing purpose, the signal can be controlled by the user as detailed in section 2.6.8.

2.5.7 MOD_ABS

Mod_ABS is pulled-down to ground in the module. The Mod_ABS is asserted “Low” when the module is inserted and it is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

2.6 ML4022-LB-V3 Specific Functions

2.6.1 Module State

The Module State describes module-wide behaviors and properties. The ML4022-LB-V3 implements two module states: ModuleReady and ModuleLowPwr.
The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the device is in Low Power mode, the Led turns into Red and the PWM is deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, the Led turns into Green and the PWM is activated. The module state encoding for ModuleReady is 011.

Page	Address	Bit	Name	Description	Type
Lower Page	**3**	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

2.6.2 Module State Transition

The state transition between Low Power and High Power is related to three parameters:

1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for Low Power and High Power state, are summarized in the table below.

ForceLowPwr (Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

2.6.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Page	Address	Bit	Name	Description	Type
Lower Page	**26**	7	IntL/TxFaultDD Control	This bit controls the output signal at pad 22, also controls which lanes reports a fault condition on pad 2 0b: pad 22 signal is IntL, and pad 2 reports Tx faults conditions for both Tx lanes (Default) 1b: pad 22 is TxFaultDD, and pad 2 reports Tx faults conditions for only lane 0	RW
		6	LowPwr	Parameter used to control the module power mode (refer to section 2.6.2) Default value =1	
		4	ForceLowPwr	0b: (default) 1b: Forces module into low power mode	
		3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=not in reset 1b=Software reset	
	3	0	Software interrupt	Digital State of Interrupt: 0b: Interrupt occured 1b: No interrupt occured	RO

2.6.4 TxFault, IntL/ TxFaultDD

TxFault and IntL/ TxFaultDD are module outputs. The ML4022-LB-V3 allows the user to control the state these signals from register 143 of page 03.

Page	Address	Bit	Name	Description	Type
Page 03h	**143**	4	TxFault control bit	1b: TxFault set High 0b: TxFault set Low	RW
		5	IntL/ TxFaultDD control bit	1b: TxFaultDD set High 0b: TxFaultDD set Low	
		TBD	IntL operation	1b: user control 0b: normal operation (Default)	

2.6.5 TxDisable, TxDisableDD

TxDisable and TxDisableDD are module inputs from the Host. User can read the digital state of these signals from register 141 of Page 03, as shown below.

Page	Address	Bit	Name	Description	Type
Page 03h	**141**	0	TxDisable	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
		1	TxDisableDD		
Page 03h		4	TxDisable	Transition Detection: Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
		5	TxDisableDD		

2.6.6 LPMode

LPMode is an input signal to the module, operating with active high logic. The LPMode signal is pulled up to Vcc in the module. The LPMode signal intervenes in the Module State Transition (refer to section 2.6.2 for more details). User can read the digital state of the LPMode signal from register 139 of Page 03, as shown below.

Page	Address	Bit	Name	Description	Type
Page 03h	**139**	0	LPMode	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
		4	LPMode	Transition Detection: Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW

2.6.7 Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module inputs. User can read the digital state of these signals from register 142 of Page 03, as shown below.

Page	Address	Bit	Name	Description	Type
Page 03h	142	0	Speed1	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
		1	Speed2		
		2	Speed1DD		
		3	Speed2DD		
		4	Speed1	Transition detection: Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
		5	Speed2		
		6	Speed1DD		
		7	Speed2DD		

2.6.8 RxLOS, RxLOSDD

RxLOS and RxLOSDD are module output signals. These signals can be controlled using two modes:

1. Following TxDisable state
2. Direct signal control

2.5.5.1 Source Control

Page	Address	Bit	Name	Description	Type
Page 03h	143	0	RxLOS control source	1b: RXLOS follows digital state of TxDisable 0b: RXLOS controlled directly through bit 1	RW
		2	RxLOSDD control source	1b: RXLOSDD follows digital state of TxDisableDD 0b: RXLOSDDcontrolled directly through bit 3	

2.5.5.2 State Control

Page	Address	Bit	Name	Description	Type
Page 03h	143	1	RxLOS State Control	1b: RXLOS set high 0b: RXLOS set Low	RW
		3	RxLOSDD State Control	1b: RXLOSDD set high 0b: RXLOSDD set Low	

2.6.9 Temperature Monitor

The ML4022-LB-V3 has an internal temperature sensor in order to continuously monitor the module temperature. The temperature sensor readings are present in low-memory registers 14-15. Internally measured module temperature is represented as a 16-bit signed two's complement value in increment of 1/256 degrees Celsius, yielding a total range of –128DegC to +128DegC that is considered valid between –40 and +125C. The location of the temperature sensor is shown below.

Page	Address	Bit	Name	Description	Type
Lower Page	14	ALL	Temperature MSB	Internally measured module temperature	RO
	15	ALL	Temperature LSB		

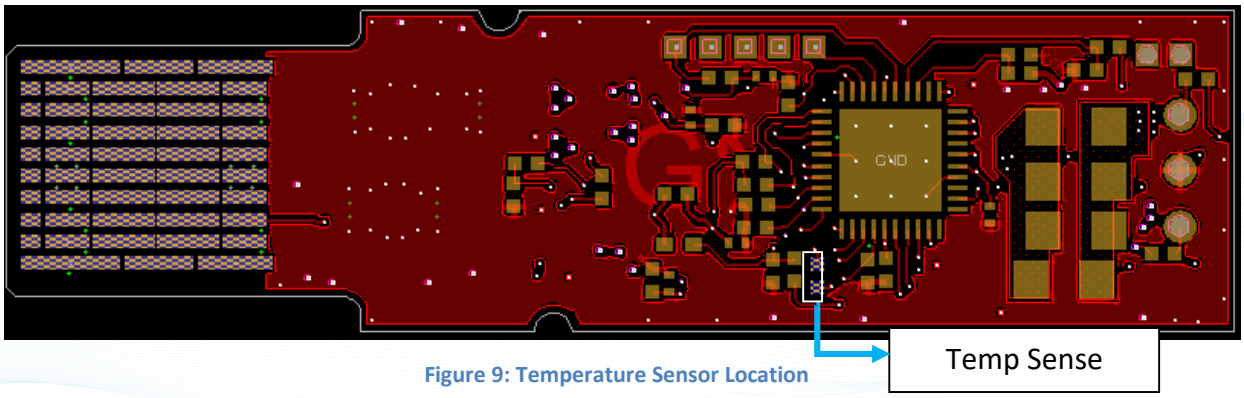

Figure 9: Temperature Sensor Location

The temperature Alarms and warnings interrupt flags exists in lower page.

Address	Address	Bit	Name	Description	Type
Lower Page	11	3	L-Temp Low Warning	Latched low temperature warning flag	RO
		2	L-Temp High Warning	Latched high temperature warning flag	
		1	L-Temp Low Alarm	Latched low temperature alarm flag	
		0	L-Temp High Alarm	Latched high temperature alarm flag	

2.6.10 Programmable Power Dissipation and Thermal Emulation

Registers 135, 136, 137 and 138, page 03h are used for PWM control over I2C. They are 8-bit data wide registers.
The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low power mode the module automatically turns off PWM. The values written in these registers are permanently stored. The PWM can also be used for module thermal emulation.
The module contains 4 thermal spots positioned where the optical transceivers usually are in an optical module that is heated relative to the related PWM register.

The maximum power dissipation and distribution differ depending on the module part number, as described in the following sections

2.6.5.1 ML4022-LB-V3

In the ML4022-LB-V3 part number, each spot is 1.08W. Programmable power can be controlled using PWM, thus allowing a power consumption that covers all the range from 0 to 4.32W with 4.2mW resolution.
Note that these values are the net spots consumption, where the module components dissipate around 0.14W, which is added to spots power to get total module consumption.

Address	Address	Bit	Name	Description	Type
Page 03h	135	7:0	PWM controller 1	1.08W Top power spot control register, powered by VccR net	RW NVR
	136	7:0	PWM controller 2	1.08W Top power spot control register, powered by VccT net	
	137	7:0	PWM controller 3	1.08W Bottom power spot control register, powered by VccR net	
	138	7:0	PWM controller 4	1.08W Top power spot control register, powered by VccT net	

In the figure below, the red spots represent the thermal spots of the ML4022-LB-V3 module.

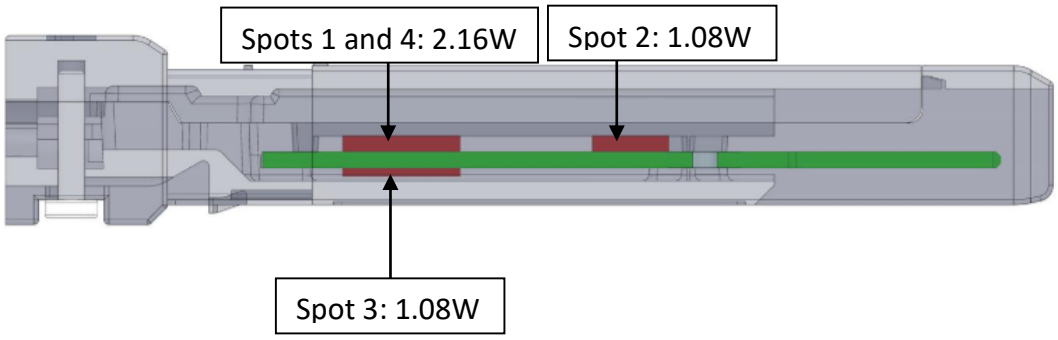

Figure 10: ML4022-LB-V3 Power Spots Location

2.6.5.2 ML4022-LB-5W-V3

In the ML4022-LB-5W-V3 part number, spots 1 and 3 are 1.4W each, and spots 2 and 4 are 1.08W each. Programmable power can be controlled using PWM, thus allowing a power consumption that covers all the range from 0 to 4.96W.
Note that these values are the net spots consumption, where the module components dissipate around 0.14W, which is added to spots power to get total module consumption.

Address	Address	Bit	Name	Description	Type
Page 03h	135	7:0	PWM controller 1	1.4W Top power spot control register, powered by VccR net	RW NVR
	136	7:0	PWM controller 2	1.08W Top power spot control register, powered by VccT net	
	137	7:0	PWM controller 3	1.4W Bottom power spot control register, powered by VccR	
	138	7:0	PWM controller 4	1.08W Top power spot control register, powered by VccT net	

In the figure below, the red spots represent the thermal spots of the ML4022-LB-5W-V3 module.

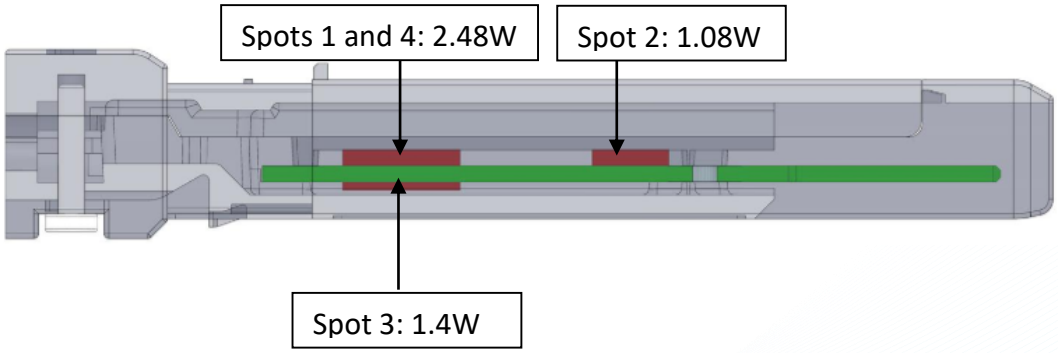

Figure 11: ML4022-LB-5W-V3 Power Spots Location

2.6.11 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module reaches the cut-off temperature, the PWM will automatically turns off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM turns on again with the same previous values.
The Cut-Off temperature for the ML4022-LB-V3 is 85 DegC and it can be programmed to any value from register 134 of memory page03. Maximum cut-off temperature is 90 DegC.

Page	Address	Bit	Name	Description	Type
Page 03h	**134**	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW

2.6.12 Voltage Sense

The ML4022-LB-V3 features two voltage sense circuits that allow measuring of internal module voltages VccT and VccR. Measured values range from 0 to 6.55V. LSB unit is 100uV.

Page	Address	Bit	Name	Description	Type
Lower Page	16	ALL	VccR MSB	Internally measured module VccR	RO
	17	ALL	VccR LSB		
	20	ALL	VccT MSB	Internally measured module VccT	
	21	ALL	VccT LSB		

The Voltage Alarms and warnings interrupt flags exists in lower page.

Page	Address	Bit	Name	Description	Type
Lower Page	11	7	L-VCCR Low Warning	Latched low supply voltage warning flag	RO
		6	L-VCCR High Warning	Latched high supply voltage warning flag	
		5	L-VCCR Low Alarm	Latched low supply voltage alarm flag	
		4	L-VCCR High Alarm	Latched high supply voltage alarm flag	

Page	Address	Bit	Name	Description	Type
Lower Page	13	7	L-VCCT Low Warning	Latched low supply voltage warning flag	RO
		6	L-VCCT High Warning	Latched high supply voltage warning flag	
		5	L-VCCT Low Alarm	Latched low supply voltage alarm flag	
		4	L-VCCT High Alarm	Latched high supply voltage alarm flag	

2.6.13 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 of Page03.

Page	Address	Bit	Name	Description	Type
Page 03h	132	All	Insertion Counter MSB		RO
	133	All	Insertion Counter LSB	LSB unit = 1 insertion	

2.6.14 Alarm and Warning Thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 01.

Page	Address	Bit	Name	Default Value	Type
Page 01h	177	ALL	high temp alarm threshold (MSB)	80˚C	RO
	178	ALL	high temp alarm threshold (LSB)		
	179	ALL	low temp alarm threshold (MSB)	0˚C	
	180	ALL	low temp alarm threshold (LSB)		
	181	ALL	high temp warning threshold (MSB)	75˚C	
	182	ALL	high temp warning threshold (LSB)		
	183	ALL	low temp warning threshold (MSB)	5˚C	
	184	ALL	low temp warning threshold (LSB)		
	185	ALL	high volt alarm threshold (MSB)	3.6 V	
	186	ALL	high volt alarm threshold (LSB)		
	187	ALL	low volt alarm threshold (MSB)	3.0 V	
	188	ALL	low volt alarm threshold (LSB)		
	189	ALL	high volt warning threshold (MSB)	3.55 V	
	190	ALL	high volt warning threshold (LSB)		
	191	ALL	low volt warning threshold (MSB)	3.05 V	
	192	ALL	low volt warning threshold (LSB)		

2.6.15 FW and HW Revision

Information about the FW and HW revision are present in lower page registers 39 and 40, and in Page 01, registers 130 and 131 as described in the table below.

Page	Address	Bit	Description	Type
Lower Page	39	All	Major FW Rev	RO
	40	All	Minor FW Rev	
Page 01h	130	All	Major HW Rev	
	131	All	Minor HW Rev	

3. High Speed Signals

SFP-DD supports two channels. High speed signals are electrically looped back from TX side to RX side of the module, every differential TX pair is connected to its corresponding RX pair, and the signals are AC coupled as specified by SFP-DD MSA HW specs. The Passive traces connecting TX to RX pairs are designed to support a data rate up to 28Gbaud (56Gbps).

4. ML4022-LB-V3 Pin Allocation

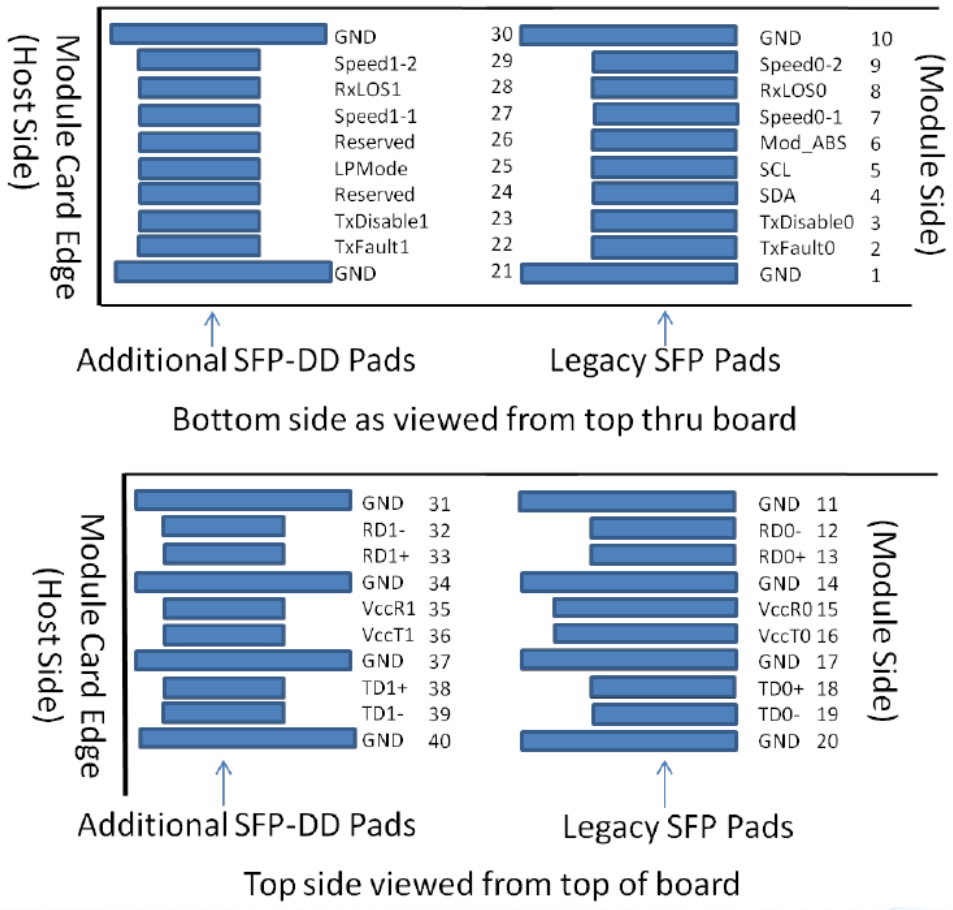

Figure 12: Module Pad Layout

Revision History

Revision number	Date	Description
0.1	2/24/2022	▪ Preliminary
0.2	2/28/2022	▪ Update section 2.6.3 ▪ Update Pin allocation in section 4